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Amendments to the Claims

Please add new claims 5- and amend the remaining claims as follows:

1. (Currently Amended) A method for fabricating a nonvolatile memory device comprising:

forming a lower insulating layer and a sacrificial layer on a semiconductor substrate;

patterning the sacrificial layer and ~~lower insulating layer, wherein~~ forming spacers ~~are formed~~ on sidewalls of the sacrificial layer pattern, the spacers ~~being formed of~~ comprising polymers resulting from the ~~etching~~ patterning of the sacrificial layer;

removing the exposed lower insulating layer using the sacrificial layer pattern and the spacers as an etching mask to form a lower insulating layer pattern; and

removing the sacrificial layer pattern and the spacers.

2. (Currently Amended) The method as defined by claim 1, wherein the sacrificial layer ~~is formed of~~ comprises a nitride.

3. (Original) The method as defined by claim 1, wherein the spacers have a width between 300Å and 1000Å.

4. (Original) The method as defined by claim 1, further comprising:

forming an upper oxide layer with uniform thickness on the lower insulating layer pattern; and

forming a gate poly on the upper oxide layer.

5. (New) The method as defined by claim 5, further comprising forming a photoresist pattern on the sacrificial layer.

6. (New) The method as defined by claim 5, wherein patterning the sacrificial layer and forming spacers comprises etching the sacrificial layer using the photoresist pattern as a mask.

7. (New) The method as defined by claim 6, wherein forming the photoresist pattern comprises irradiating the photoresist with a source of light having an i-line wavelength.

8. (New) The method as defined by claim 6, wherein the etched region of the sacrificial layer pattern has narrower linewidth than that defined by the photoresist pattern

9. (New) The method as defined by claim 7, wherein an etched region of the sacrificial layer pattern has a narrower linewidth than that defined by the photoresist pattern.

10. (New) The method as defined by claim 1, wherein removing the exposed lower insulating layer comprises wet etching the exposed lower insulating layer.

11. (New) The method as defined by claim 10, wherein a region removed from the lower insulating layer pattern has a narrow linewidth relative to removing the exposed lower insulating layer using the sacrificial layer pattern alone as an etching mask.

12. (New) The method as defined by claim 8, wherein removing the exposed lower insulating layer comprises wet etching the exposed lower insulating layer.

13. (New) The method as defined by claim 12, wherein an etched region in the lower insulating layer pattern has a linewidth not broader than a linewidth defined by the photoresist pattern.

14. (New) The method as defined by claim 1, wherein the method increases a coupling ratio of the nonvolatile memory device relative to a method that removes the exposed lower insulating layer using the sacrificial layer pattern alone as an etching mask.

15. (New) The method as defined by claim 2, wherein the lower insulating layer comprises an oxide.

16. (New) The method as defined by claim 1, further comprising forming a tunnel oxide on the semiconductor substrate.

17. (New) The method as defined by claim 16, further comprising forming a gate poly layer on the tunnel oxide.

18. (New) The method as defined by claim 6, wherein the spacers are formed of polymers resulting from the etching of the sacrificial layer.